Code: 9A10504 R09

B.Tech III Year II Semester (R09) Supplementary Examinations December/January 2014/2015

LINEAR & DIGITAL IC APPLICATIONS

(Common to EEE & MCT)

Time: 3 hours Max. Marks: 70

Answer any FIVE questions

All questions carry equal marks

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1 (a) Derive the expression for voltage gain, input resistance and output resistance of dual input balanced output differential amplifier.
(b) Classify integrated circuits based on their packages and temperature ranges.
(c) Elaborate the concept of virtual ground in op-amp.

2 (a) Draw the circuit diagram of astable multivibrator using an op-amp and explain its operation. Mention any two applications.
(b) Discuss about log amplifier and mention its applications.

3 (a) Draw the functional schematic of 555 timers and describe in detail how this IC can be used to realize a monostable multivibrator.
(b) Describe how a PPL IC can be used for implementing amplitude and frequency demodulations.

4 (a) Draw the circuit for CMOS OR-AND-Invert (OAI) logic gate and explain its functioning clearly with the help of functional table.
(b) Draw the resistive model of a CMOS inverter and explain its behavior for LOW and HIGH outputs.

5 (a) Explain sinking current and source current of TTL output. Which of the above parameter decide the fan-out and how?
(b) What are the precautions to be taken while handling CMOS logic gates?

6 (a) What is the importance of time dimension in VHDL and explain its function?
(b) Write a VHDL program in behavioral style to generate a clock with off time and on time equal to 10ns.

7 (a) Design 1:8 demultiplexer using two 1:4 demultiplexer.
(b) Explain the top-level design of ALU using VHDL with its function table.

8 (a) Differentiate between a latch and flip-flop.
(b) Design a 3-bit binary synchronous counter.
(c) With the help of the master-slave type S-R flip-flop explain how edge triggered operation becomes possible.

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